28nm CPI (Chip/Package Interactio&

28nm CPI (Chip/Package Interactions) in Large Size eWLB (Embedded Wafer Level BGA) Fan-Out Wafer Level Packages

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***Abstract*— To meet the continued demand for form factor reduction and functional integration of electronic devices, Wafer Level Packaging (WLP) is an attractive packaging solution with many advantages in comparison with standard Ball Grid Array (BGA) packages. The advancement of fan-out WLP has made it a more promising solution as compared with fan-in WLP, because it can offer greater flexibility in enabling more IO's, multi-chips, heterogeneous integration and 3D SiP. In particular, Embedded Wafer Level BGA (eWLB) is a fan-out WLP solution which can enable applications that require higher input/output (I/O) density, smaller form factor, excellent heat dissipation, and thin package profile, and it has the potential to evolve in various configurations with proven integration flexibility, process robustness, manufacturing capacity and production yield. It also provides integration of multiple dies vertically and horizontally in a single package without substrates.**

For eWLB fan-out WLP, the structural design as well as selection of materials is very important in determining the process yield and long term reliability. Therefore it is necessary to investigate the key design factors affecting the reliability comprehensively. Th

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based on these finite element analysis (FEA) simulation results, the BEOL stack with the highest CPI risk is chosen for package reliability testing using the CPI test vehicle (TV).
In this work, we assess production readiness for large body size multilayer RDL based eWLB packages through;

- Functional test of 28nm circuits
- Reliability test
- Electrical and thermal characterization
- Thermo-mechanical characterization and simulation

Advanced Wafer-Level Technology: eWLB/FOWLP

eWLB package technology is based on an embedded device technology with fan-out redistribution. The thin-film redistribution layer (RDL) of the eWLB enables very flexible and highly customizable package designs. The length of the redistribution lines is in the range of the die size[5].
eWLB has the ability to attain minimum interconnection length and excellent electrical performance. In a few cases, eWLB achieved a 20~40% reduction in package size a over 50% volume reduction as compared to other packagi solutions such as flipchip or wirebonding packages due its slim and smaller form factor. For radio frequency (R and high-frequency microwave or mmWave devices, significantly improvements in overall device performar was illustrated by eWLB, which showed less parasi electrical interference.



Figure 2. Key features of advanced eWLB/FO–WL Innovative and high performance solution of integration

II. EXPERIMENTAL WORKS

Test Vehicle Specification

The three different test vehicles were designed w 10x10-15x15mm package sizes and multi-layer RDL. A those test vehicles were assembled and packaged with t

Reliab

For component level reliabi
were assembled with daisyc
devices. Table 2 shows the
conditions in this study.

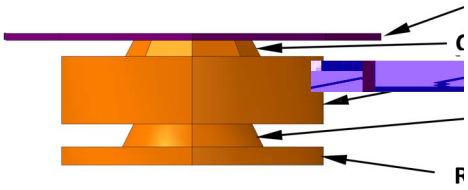
All tested eWLB parts testec
package level and board
successfully. eWLB with
passed JEDEC TC-B conditic
cycling (TC) reliability test.
body thickness, it passed 10(
300 drops, no failure has
performance was robust

Table 2. Package & Board
eWLB with advanc

Test	
PC Pre-Cond	
TC Temp. Cycling	
HTSL, High Temp Storage Life	
THS, Temp Humidity Storage	
TCoB	
Drop Test	

RDL Via Shap

RDL via shap
advanced node
adopted to ev
interconnect st
BEOL layer in
4 shows a RD
different RDL
tapered via, wl
Other variation
and 4 are for a
and a thick Cu
a thin Cu pillar
of the FEA mc
250°C to -55°
normalized ma
different via s
conditions are



Option 4: Via with Thin Cu Column

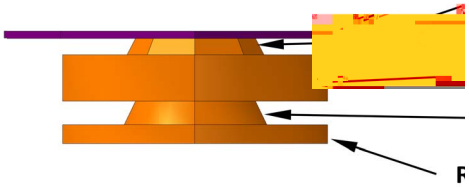


Figure 5. Design options of RDL via interconnection structur

Table 3. Normalized Max. Principal Stress.

Temperature (°C)	Design Opti		
	1	2	
250	1.00	0.91	
125	1.00	0.93	
25	1.00	0.88	
-55	1.00	0.92	

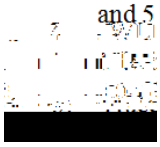
Thermal Characterization

For thermal characterization, the te4c0 0.001 0 0 10.02 224.64 128.8-792 reW nq57.36 0 0 42.54 171.48 677.52 cm/Im59 DoQBT prepared with thermal die having thermal block. Test vehicle specification was sa Table 2(b). The effect of die thickn investigated with 3 different die thicknesses and 400um. For the comparison study, sa the flip chip package were prepared.

To easily detect the temperature at th die with applied power, all test vehicles with a transistor and heating circuit bl temperature sensor. After surface mount te on a JEDEC standard 8-layer thermal tes board (PCB), 2.0W power was applie temperature was measured with thre thicknesses. As evident in Fig. 6, eWLI improvement in thermal performance fo thickness as compared to flipchip package can use a die that is thicker than flipc embedding, achieving a more than 25%

In this work, main findin

1. High-
   matcl
2. Trace
3. Trace
   and 5



Using computer simulati
electromagnetic field solver,
eWLB and flipchip package
HFSS software, the S-paran
were extracted. Table 4 illus
were compared with RLC pa
For eWLB, it w
and resistance
to its shorter
without bump
with previous r

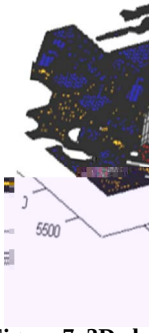


Figure 7. 3D ele

Table 4. Comp
c

Net	Inc
	flipchi
1	1.77
2	2.03
3	1.51
4	1.08